

S/N 08/650,719



PATENT

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Jeffrey S. Mailloux et al. Examiner: Hong Kim  
Serial No.: 08/650,719 Group Art Unit: 2751  
Filed: May 20, 1996 Docket: 303.623US1  
Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE  
SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

**PRELIMINARY AMENDMENT**

Assistant Commissioner for Patents  
Washington, D.C. 20231

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**IN THE CLAIMS**

Please amend claim 50 as follows:

50. (Amended) A system comprising:
- a microprocessor;
  - a memory, coupled to the microprocessor, the memory [in] selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and
  - a system clock coupled to the microprocessor.

Please add new claims 59-64 as follows:

59. (New) A method for accessing a storage device, comprising:
- receiving a first address to the storage device; ROW ADDRESS
  - receiving a burst/pipeline signal;
  - selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;
  - obtaining a second address to the storage device; and COL ADDRESS
  - accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

ROW  
ADDR

COL ADDR